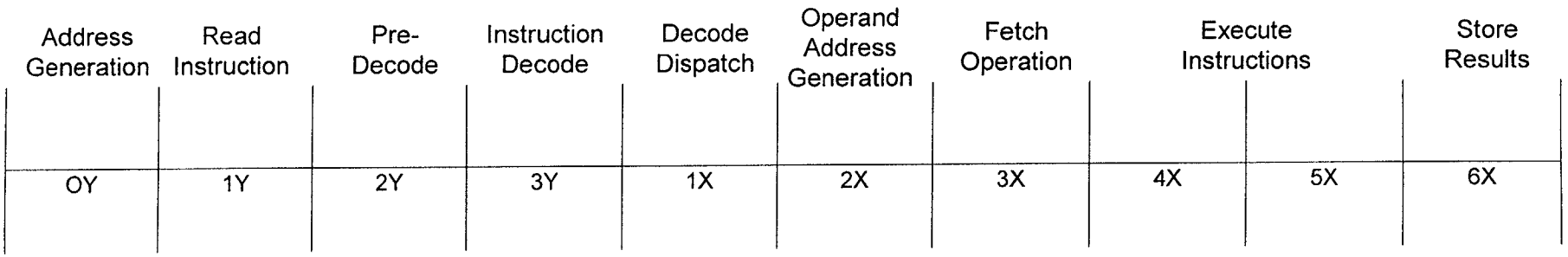

Address Generation
Read Instruction
Pre-Decode
Instruction Decode
Decode Dispatch
Operand Address Generation
Fetch Operation
Execute Instructions
Store Results
OY
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X

FIG. 1

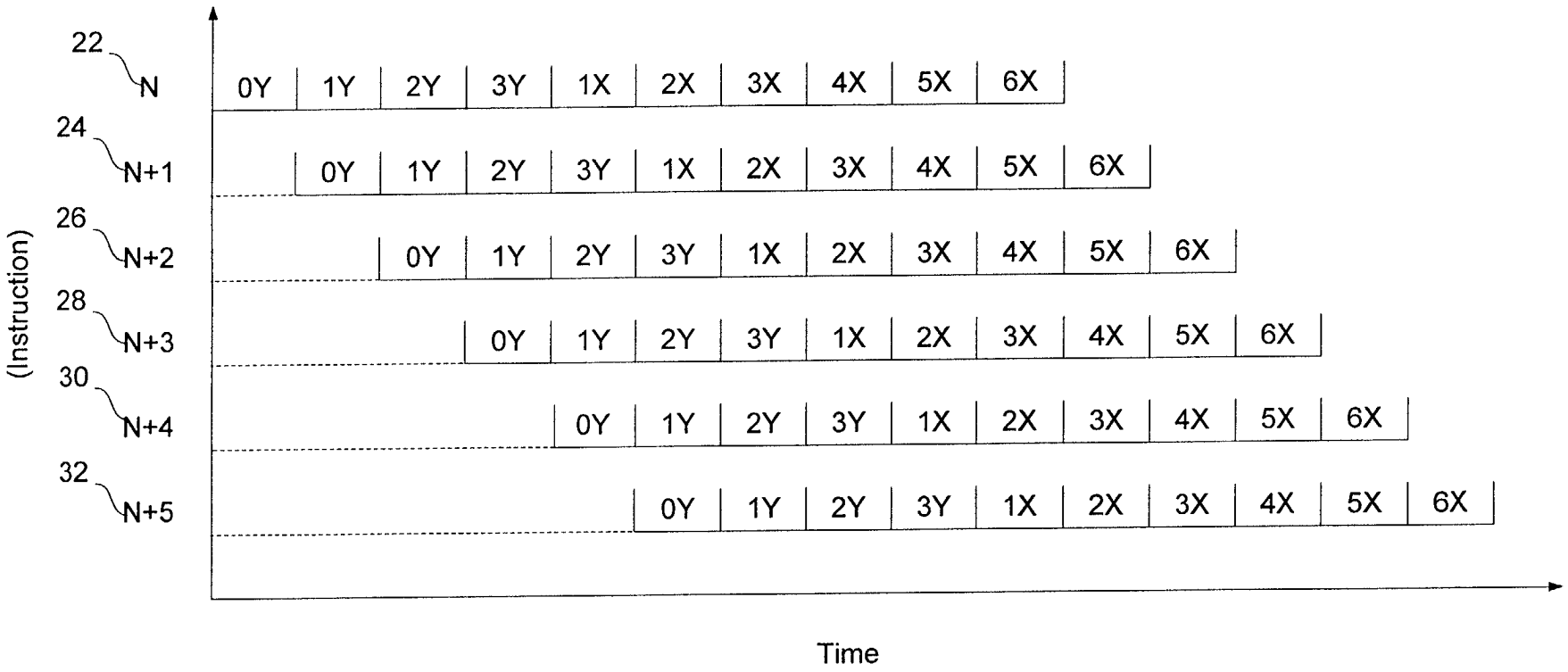

22
N
0Y 1Y 2Y 3Y 1X 2X 3X 4X 5X 6X
24
N+1
0Y 1Y 2Y 3Y 1X 2X 3X 4X 5X 6X
26
N+2
0Y 1Y 2Y 3Y 1X 2X 3X 4X 5X 6X
28
N+3
0Y 1Y 2Y 3Y 1X 2X 3X 4X 5X 6X
30
N+4
0Y 1Y 2Y 3Y 1X 2X 3X 4X 5X 6X
32
N+5
0Y 1Y 2Y 3Y 1X 2X 3X 4X 5X 6X
(Instruction)
Time

FIG. 2

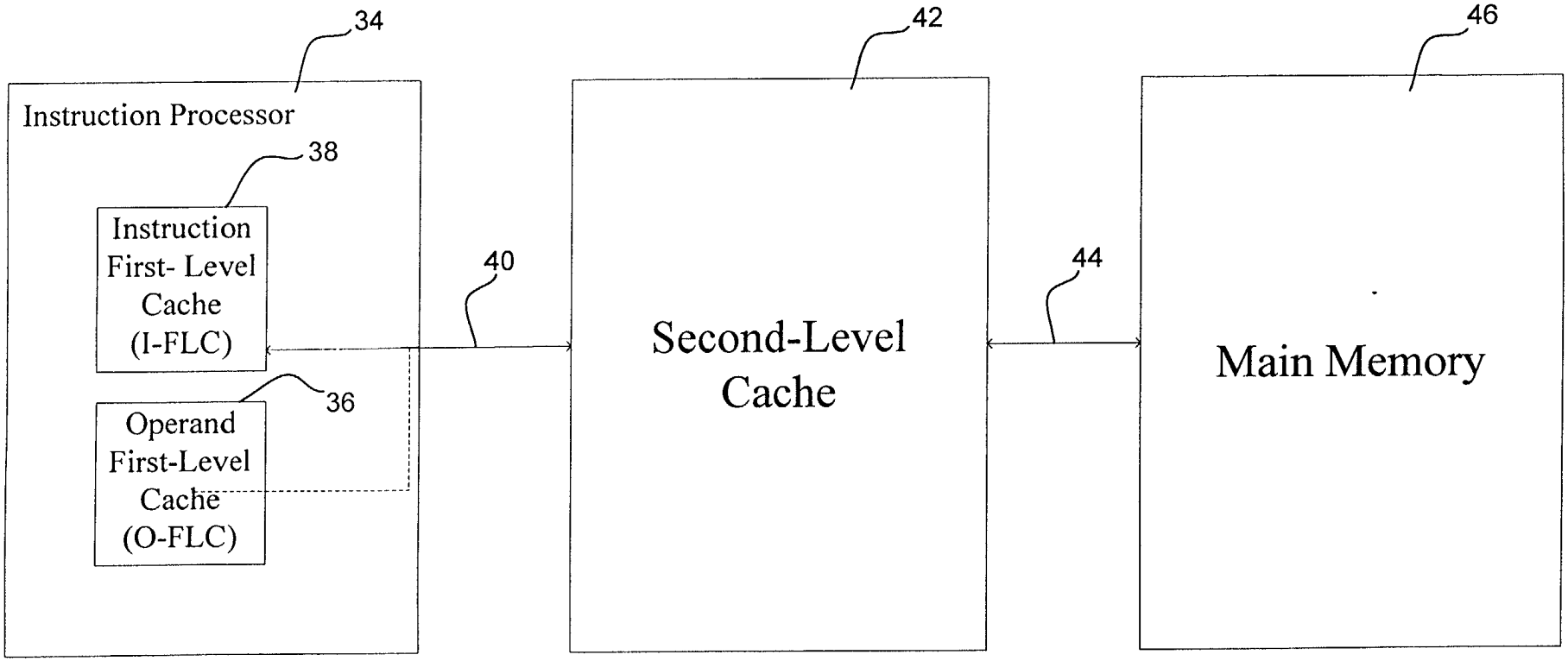

34
Instruction Processor
38
Instruction First- Level Cache (I-FLC)
36
Operand First-Level Cache (O-FLC)
40
42
Second-Level Cache
44
46
Main Memory

FIG. 3

Datasheet 4423460

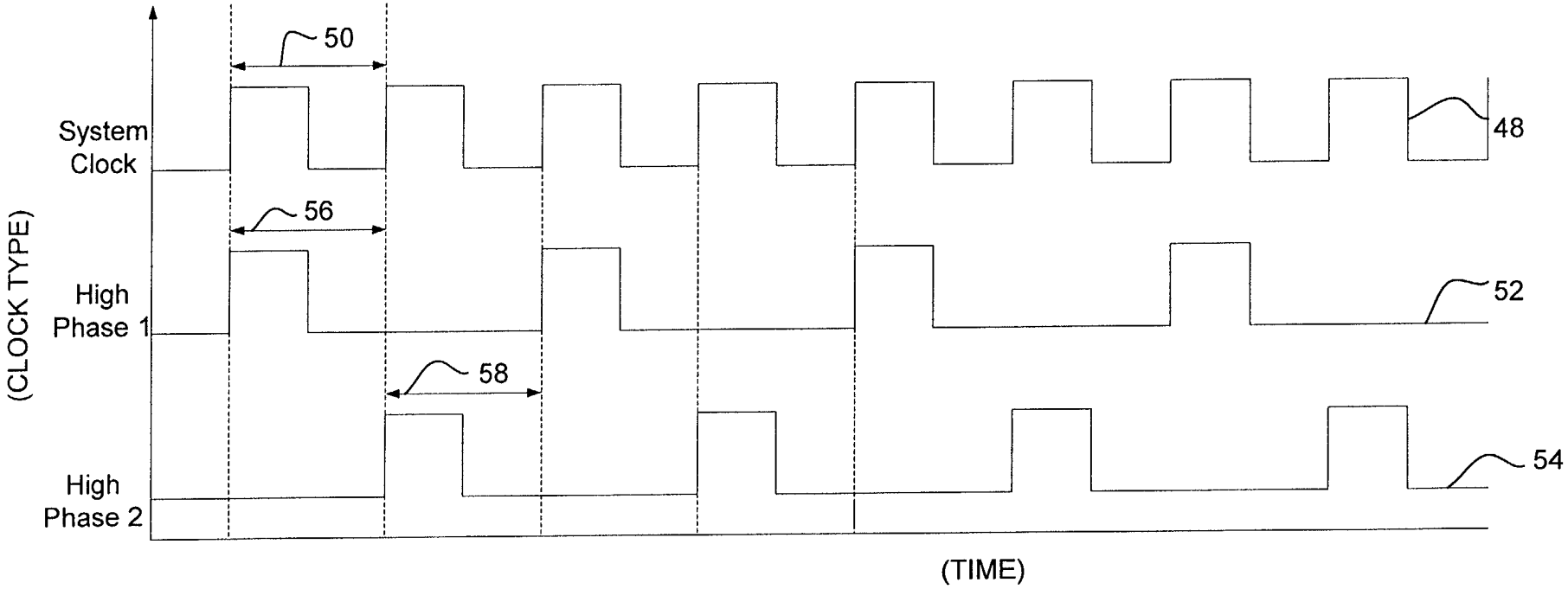


FIG. 4

Docket: HA220269

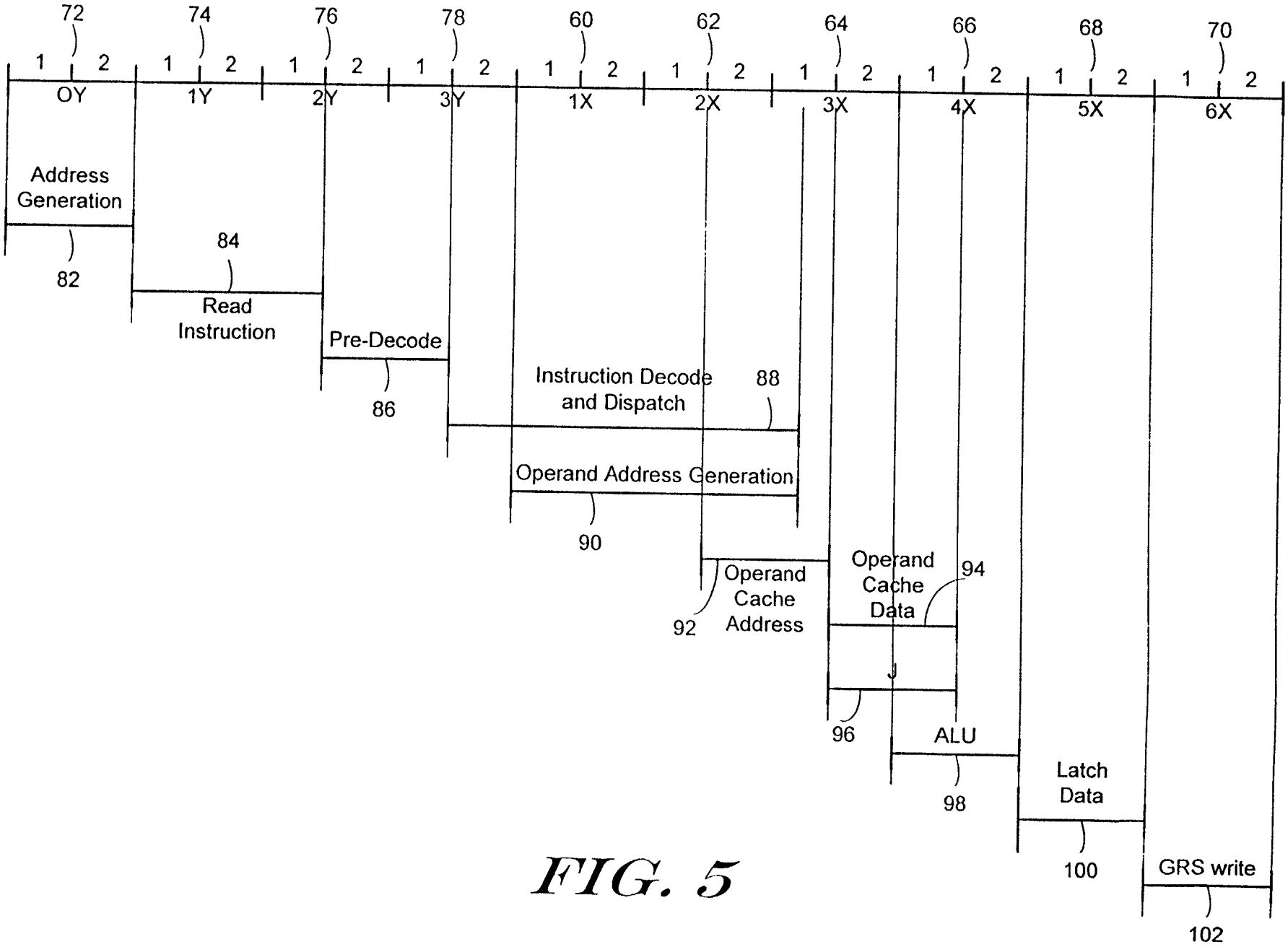


FIG. 5

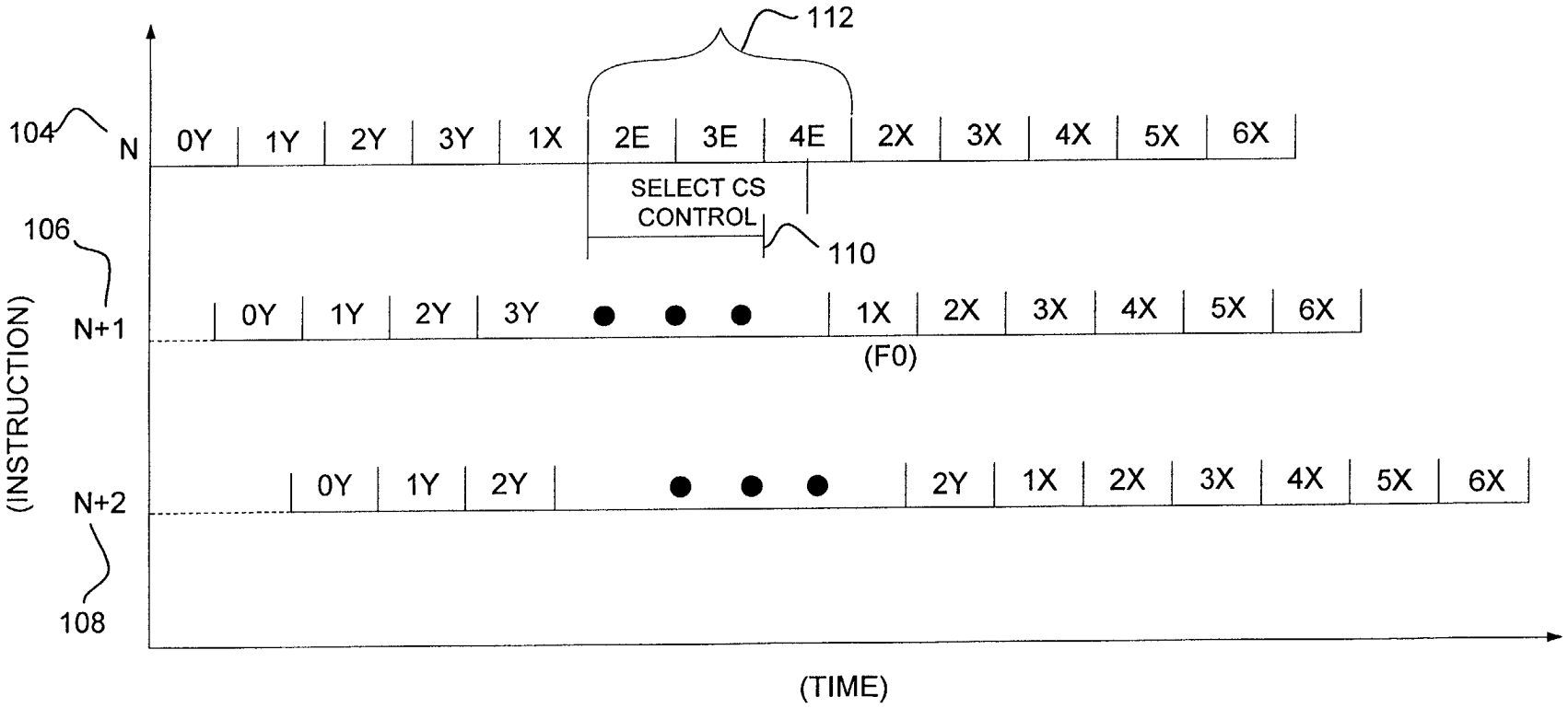
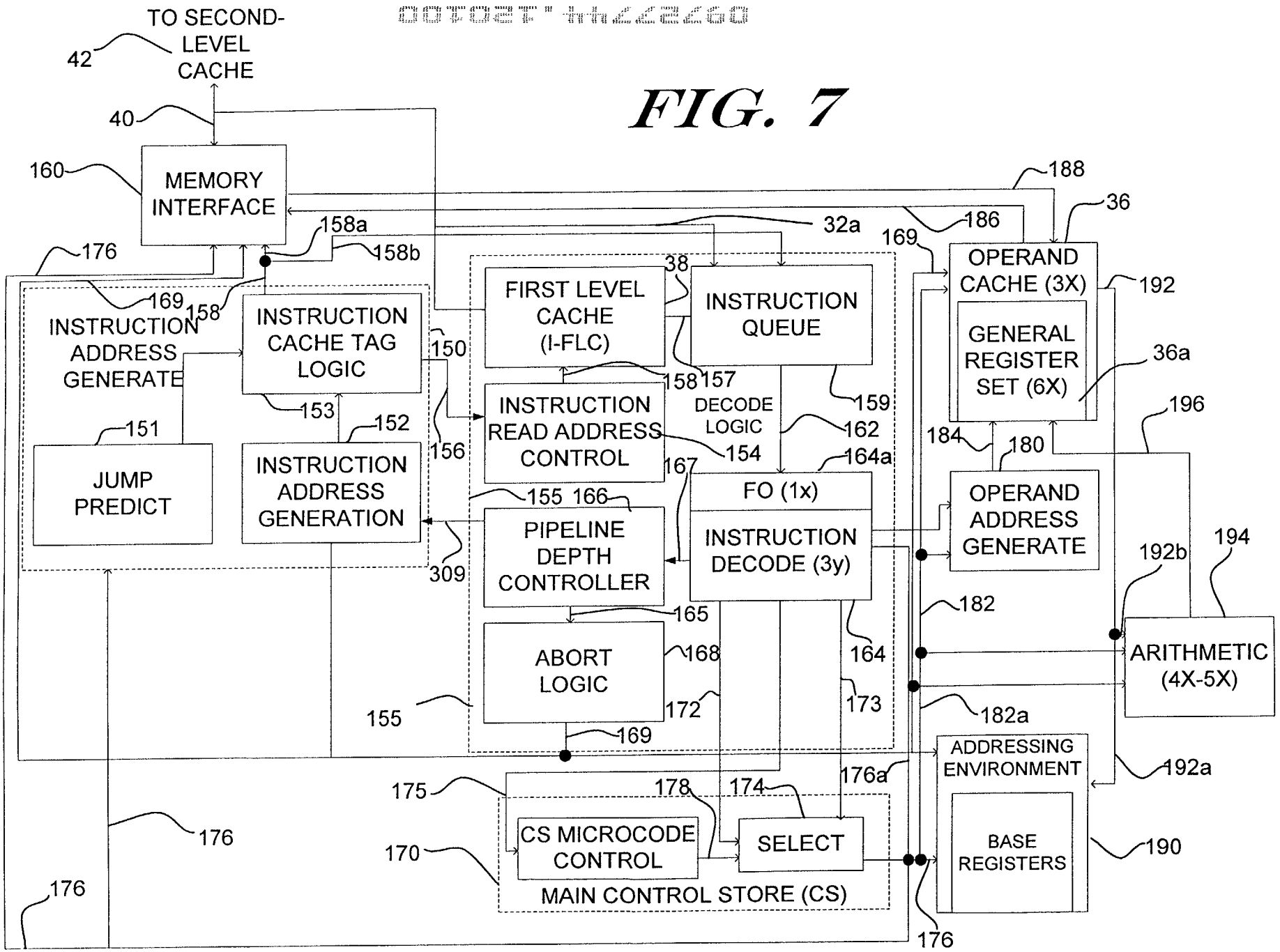

112
104
N
0Y
1Y
2Y
3Y
1X
2E
3E
4E
2X
3X
4X
5X
6X
SELECT CS CONTROL
110
106
N+1
0Y
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X
(F0)
(INSTRUCTION)
N+2
0Y
1Y
2Y
2Y
1X
2X
3X
4X
5X
6X
108
(TIME)

FIG. 6

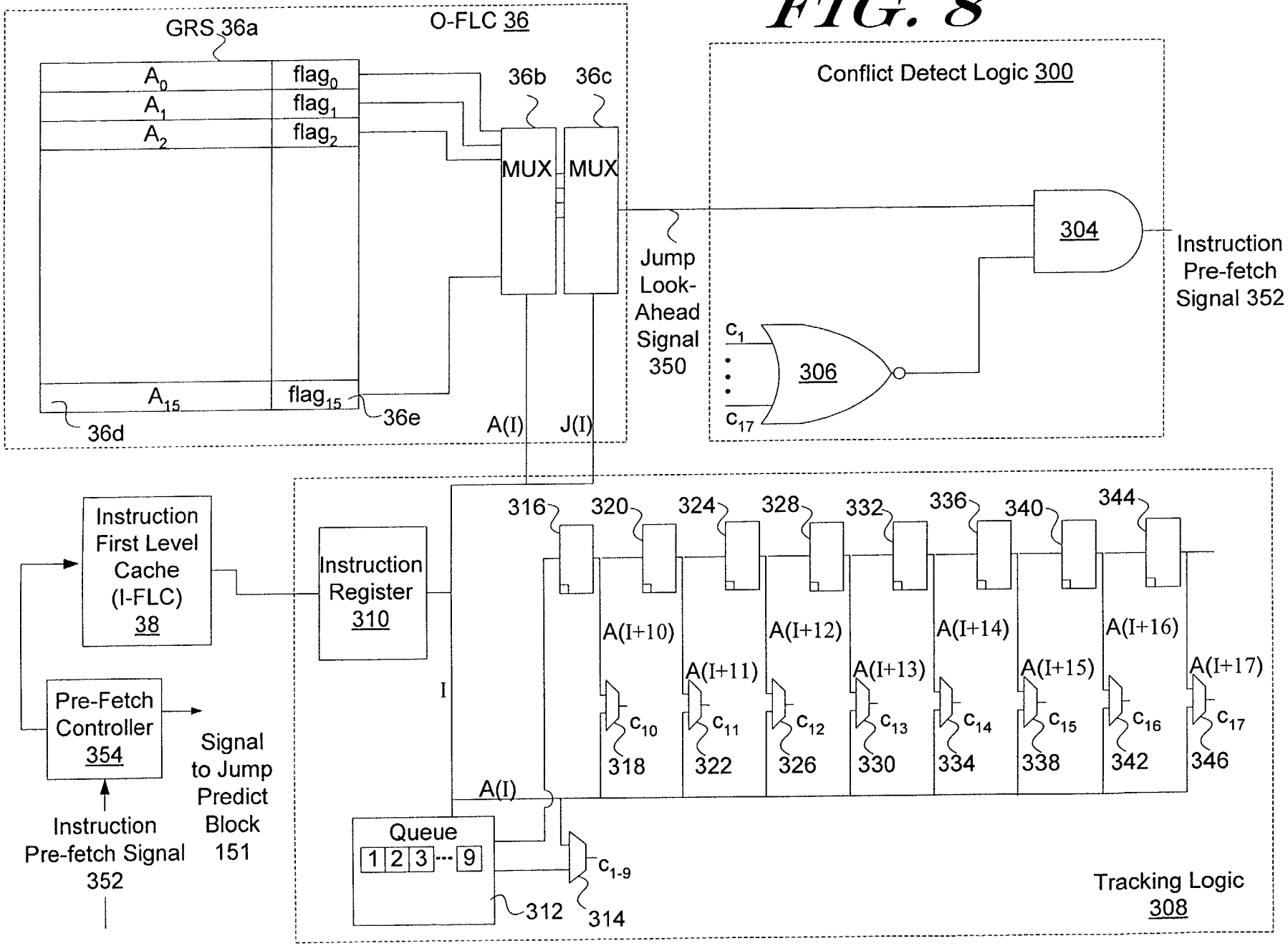
DOCKET NO. 42390

FIG. 7



DOCKET NO. 42390

FIG. 8



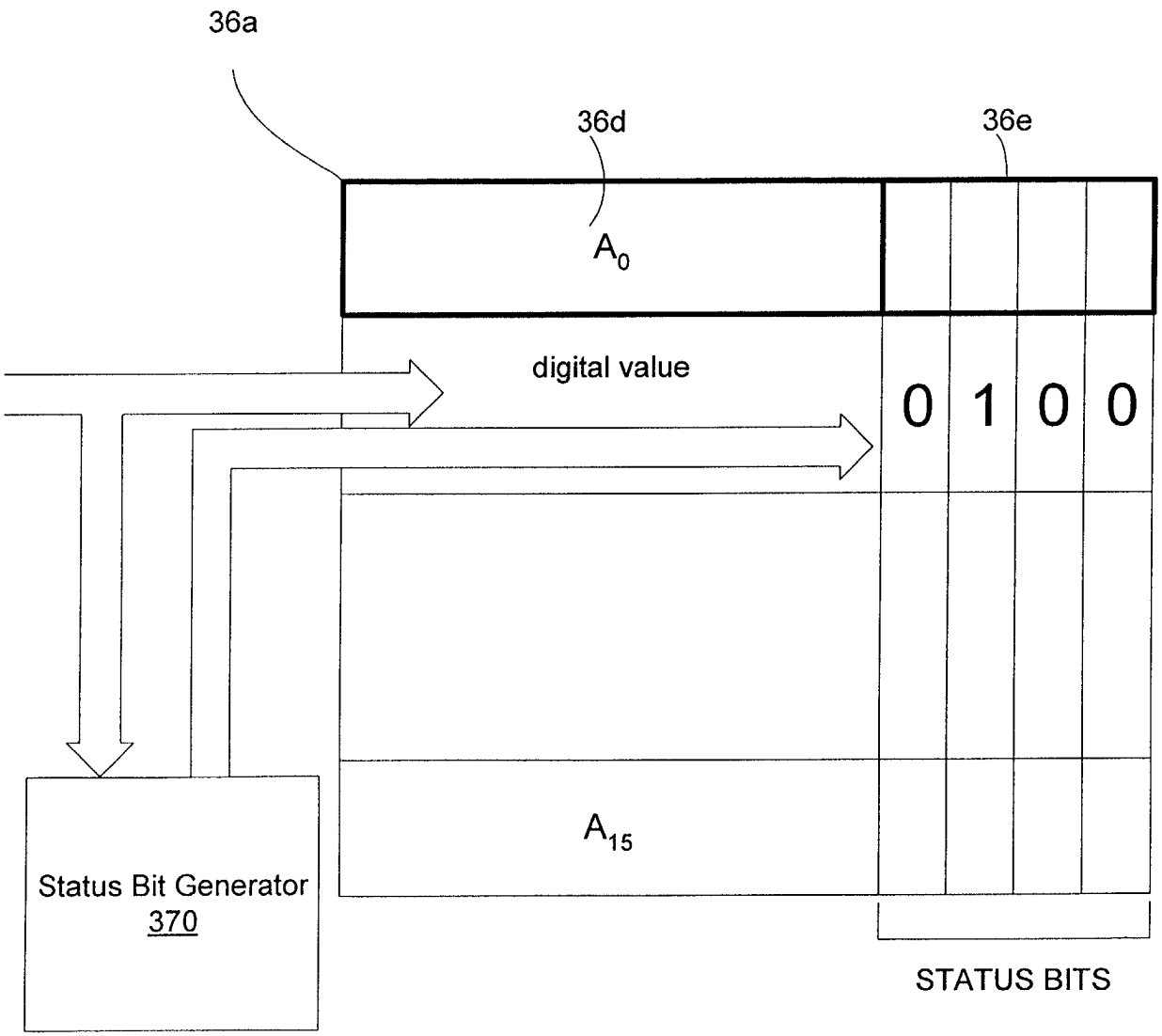

36a
36d
36e
A_0
digital value
0 1 0 0
A_{15}
Status Bit Generator
370
STATUS BITS

FIG. 9